Current Differential Line Protection Setting Considerations

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Abstract

The most common pilot line protection today is directional comparison by use of distance relays. However, the increased availability of digital communications channels has renewed the interest in line differential relaying. Current-only relays have many advantages. One of the most significant advantages is the simplicity of the scheme with regards to settings.

The percentage differential principle originally developed for transformer and generator protection was extended for use on short transmission lines already in the 1930s, and is still widely in use. These Pilot Wire Relays typically use a telephone type pilot wire channel to exchange analog information between the line terminals. The electromechanical pilot wire relays were very easy to set; they either came with factory default fixed sensitivity or had a few tap settings. What tap to use was determined by estimated fault current on the line, making sure that the relay sensitivity was sufficient for the relays to dependably trip for all types of fault on the line. Three phase sensitivity was often limited to current above load levels in order not to trip for open pilot wires.

For digital current differential line relays, the sound and simple setting principles utilized for pilot wire relays seem to have been forgotten. Commonly, the most sensitive setting (10 – 20 % of nominal current) is applied and even recommended without any consideration of actual fault current levels for the application. This practice contradicts fundamental relaying principles that balance security, sensitivity, dependability and operating speed of the protection scheme. For sensitivity, the requirement is to set the relay to detect all faults on the line with a sufficient margin, seldom does this require the most sensitive setting. Higher sensitivity will increase dependability, but decrease security. Too high sensitivity may cause false trips due to ct errors at external faults with high fault currents, or even false trips on load for channel delay measurement errors due to unequal transmit and receive delays.

This paper reviews the basic setting criteria for current differential line protection, and the charge comparison relay in particular. While setting parameters will differ depending on the type of current differential relay, the setting principles and system conditions to consider remain largely the same. Operating time, sensitivity, dependability and security requirements are examined for typical applications. Considerations for weak feed conditions, ct errors and ct saturation, and charging current are discussed. In addition, the effect of channel delay compensation errors and asymmetrical channel delays possible on digital communications networks with regards to setting considerations is examined.

Pilot Line Protection

There are two main groups of pilot protections; current comparison relays and directional comparison by use of distance relays or other directional elements. Current comparison is the term used in the PSRC “Guide for Protective Relay Applications to Transmission Lines” for all types of line differential relays using current-only as the main operating criteria.

While all line differential relays have similarities, measuring principles may differ. The term "Current Differential" is generally applied for both Pilot Wire Relays and Digital Current Differential Relays. Phase Comparison relays are line differential relays mainly intended for used with Power Line Carrier.

One main difference between the Pilot Wire Relay and the digital Current Differential Relay is the communication medium used. Pilot Wire Relays operate over an analog circuit such as a metallic pilot wire. Most digital Current Differential Relays require a digital channel (fiber optic or multiplexed). There are exceptions in both groups; digital current differential relays operating over analog channels (audiotone) and pilot wire relays operating over a digital channel via an interface.

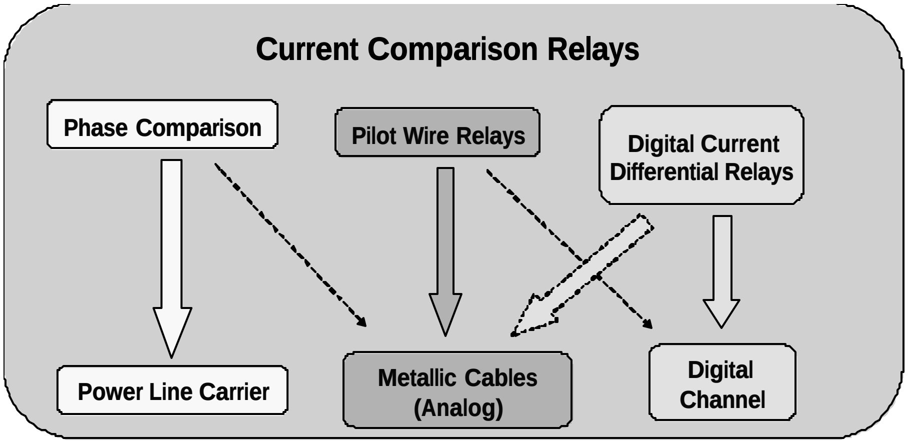


Figure 1. Current Comparison Relays with Associated Communication Media

Current Differential Line Protection

Current differential relaying is a method of extending the benefits of differential protection as applied to transformers, buses or generators to the protection of transmission lines. Comparing current flowing into a line to the current flowing out of the same line allows for a simple protection scheme with high sensitivity and high speed simultaneous tripping of both line terminals. At the same time, the differential scheme is unaffected by external effects such as faults, load and power swings.

The differential current can be measured with different methods:

- Magnitude comparison
- Phase comparison
- Phasor comparison (magnitude and angle)
- Charge comparison
- Combinations of the above

Regardless of the method used, all line differential relays operate on a difference in current into the line compared to the current out of the line.

For an internal fault, the current will flow into the line from both line terminals, with the polarity of the current transformers as shown in Figure 2. The local current I_L will be practically in phase with the remote current I_R. A small phase difference between the two currents is caused by different source angles at the local and remote end.

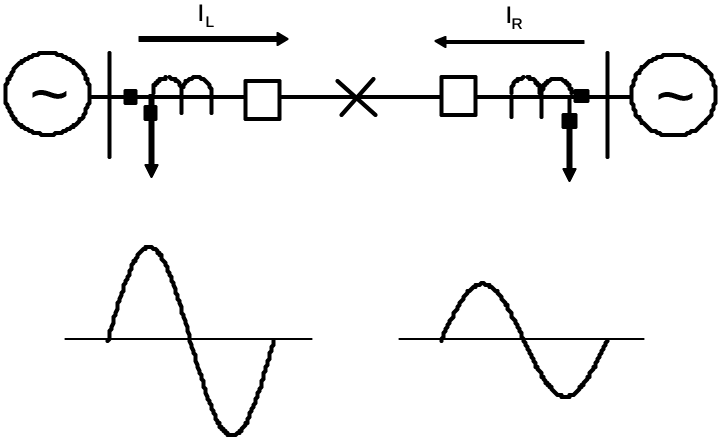


Figure 2. Internal Fault

For an external fault, the current will flow into the line in one terminal and out of the other as shown in Figure 3. The local current I_L will be 180 degrees out of phase with the remote current I_R and they will be of equal magnitude.

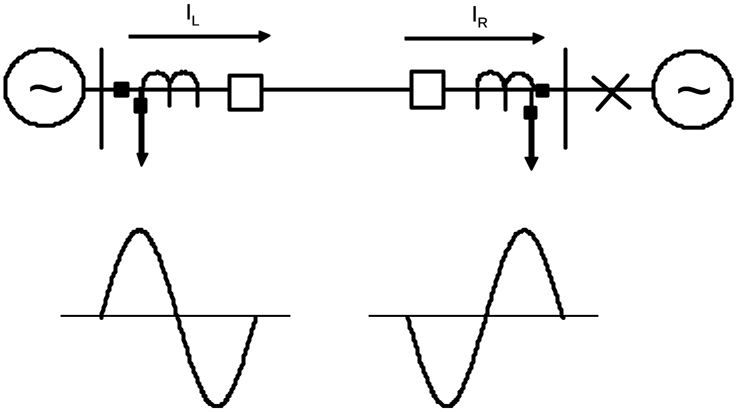


Figure 3. External Fault

To determine if a fault is on the line or outside the protected line section, it would be possible to examine just the differential current. For an internal fault:

$$\left|\overline{I}_L + \overline{I}_R\right| \neq 0 \tag{1}$$

For an external fault:

$$\left|\overline{I}_L + \overline{I}_R\right| = 0 \tag{2}$$

This simple comparison makes a differential relay very attractive for line protection as it provides a high degree of sensitivity for internal faults combined with high security for external faults.

Common to all line differential relays is the need of a reliable communications channel. A remote quantity containing the current information needs to be transferred to the local end for comparison to the local current. The quantities to be compared have to be time-coincident and the magnitude and angle information of the remote current must be preserved.

The first current differential relays used pilot wires. The pilot wire was a two conductor circuit capable of transmitting 60 Hz and dc quantities. To limit the communications requirement to a single circuit, the three phase currents were reduced to a single representative quantity. A typical voltage balance relay is shown in Figure 4. An external fault or load current produces voltages of opposite polarities over the pilot wire at the two line ends, and the resulting voltage over the operating coil is 0. For an internal fault with infeed from both line terminals, the voltage is of the same polarity and the resulting voltage causes operation of the operating coil.

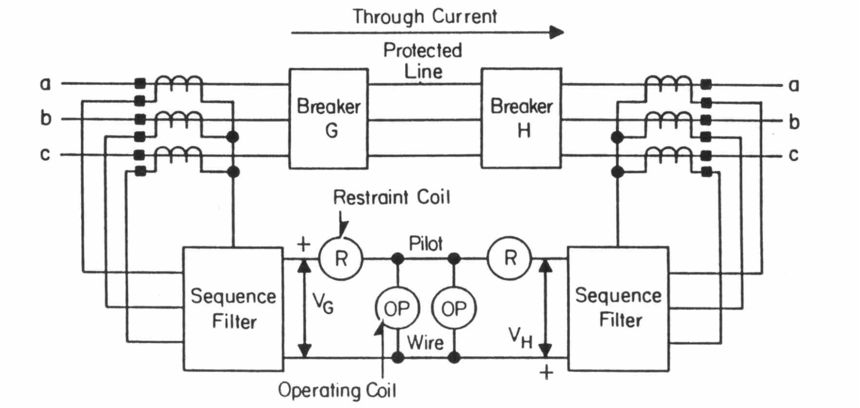


Figure 4. Pilot Wire Relay

Most digital current differential relays emulate the pilot wire relays operating principle but more complexity is added due to differences in the communication medium. While the pilot relay does its comparison in real-time, a digital current differential relay needs to compensate for the delay introduced by the communications channel for transmitting the digitized current information from one line terminal to the other.

In addition, the characteristics of the communications channel need to be taken into account both by the relay's communications interface design and the measuring principle used. The communications interface has to block a corrupted data message from being delivered to the relay and ensure that the two relays remain synchronized to each other. Accurate channel time delay measurement has to be performed so that proper alignment of the measuring quantities can be made. The relay's measuring principle needs to properly handle errors introduced by any asymmetric channel delay (different transmit and receive paths) on switched communications networks in addition to deal with power system issues causing false differential currents; ct errors and charging currents.

Current Differential Line Protection Operating Criteria

Under ideal measuring condition, the differential current carries sufficient information to distinguish between an internal and an internal fault. However, measuring errors due to different ct characteristics in the two line ends, channel delay measurement, and finite sampling frequency in the digital relays will cause the relays to measure false differential currents for non-fault conditions. The differential current therefore needs to be provided with an operating threshold. In order not to make the protection unnecessarily insensitive for low fault currents, most relays have a current dependant threshold by the use of a percentage differential characteristic.

In most differential relays, the bias (trip point) is not a fixed value but calculated from a starting point with a curve that increases as current increases. This automatic increase in the trip point allows for errors in the relay system that is proportional to the current level. Such effects include ct measuring errors and analog circuitry errors.

The pilot wire relay uses a summation transformer (or filter) to reduce the three phase currents into one representative quantity. Digital current differential relays generally perform the current differential measurement on a per phase basis and may include a ground differential element with higher sensitivity for high resistive ground faults.

While the actual measuring algorithm varies between relays of different make, most of them form one operating quantity and one restraint (bias) quantity and compare these with set thresholds.

The operating current is typically the sum of the local and remote current:

$$\left| \overline{I}_L + \overline{I}_R \right| = I_{differential} \tag{3}$$

The restraint quantity is typically a function of the total current, where the function often is a constant, k:

$$k\left(\left|I_L\right| + \left|I_R\right|\right) = I_{restraint} \tag{4}$$

Most relays also have a minimum operating current so that the operating criterion is:

$$I_{differential} > I_{min} + I_{restraint} \tag{5}$$

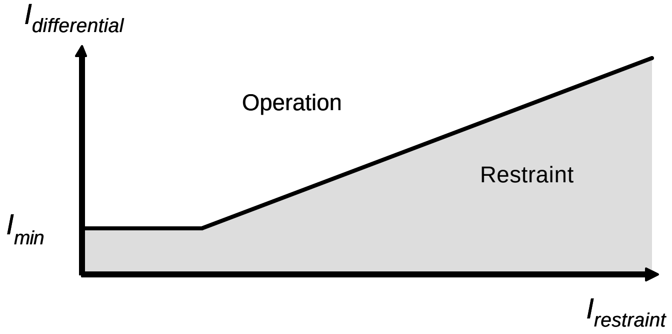


Figure 5. Percentage Restraint Characteristic

A typical percentage restraint characteristic is shown in Fig 5. The minimum operating current (I_{min}) is a settable threshold. The slope (k) may be fixed or settable. Some modern relays have two slope settings, increasing the restraint for high fault currents. The percentage differential characteristic has the advantage of providing high sensitivity for low fault currents and good security for higher fault current levels where ct errors may be larger.

Charge Comparison Current Differential Relay

One current differential measuring method is the Charge Comparison principle. The charge comparison relay was invented in 1992 to provide current differential relaying over digital switched networks. An analog (audiotone) interface is also available.

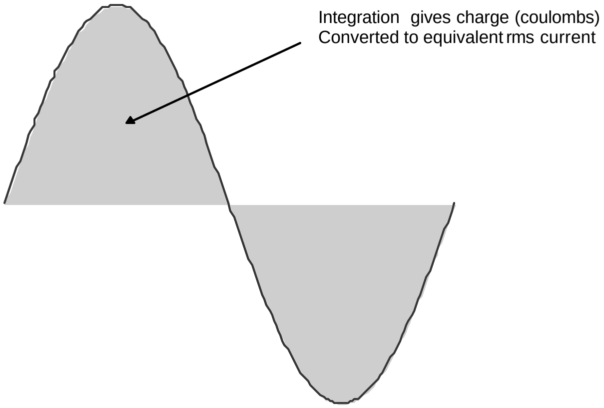


Figure 6. Integration of Current Samples to Compute Charge

To perform charge comparison, the current wave of each phase and residual is sampled every ½ ms. The half-cycle area under each wave is measured by integrating current samples between zero-crossings. For each phase and ground, the resulting ampere-seconds area (coulombs of charge) is stored in local memory, along with polarity and start/finish time tags. This storage operation occurs only if the magnitude exceeds 0.5 A rms equivalent and the half-cycle pulse width is larger than 6 ms, but does not exceed 10 ms.

Every positive (negative for 3I0) magnitude is transmitted to the remote terminal, along with phase identification and some timing information related to the pulse width. When the message is received at the remote terminal, it is assigned a received time tag. A time interval representing the channel delay compensation is then subtracted from the received time tag. The adjusted received time tag is then compared with the locally stored time tags looking for a coincidence, or a ‘nest’.

A nest is achieved when the adjusted received time tag falls between the local start and finish time tags, for a given half-cycle stored in memory.

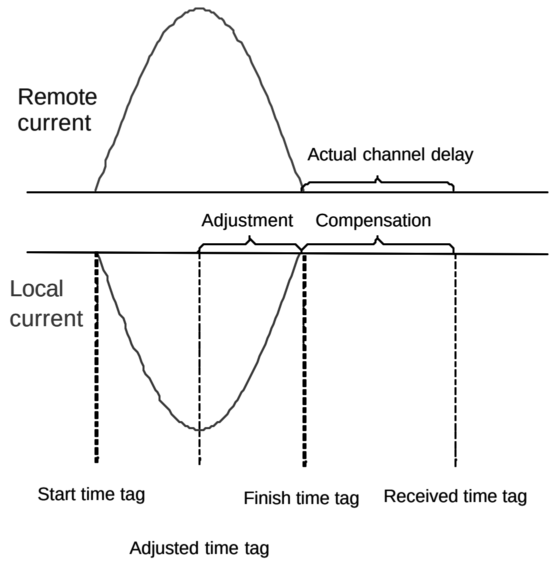


Figure 7. Charge Comparison (External Fault)

When the nesting operation is successful, the local and remote current magnitudes (actually charges converted to equivalent currents) are added to create the scalar sum (sum of absolute magnitudes) and arithmetic sum (absolute magnitude of the sum of the signed magnitudes). The scalar sum becomes the effective restraint quantity and the arithmetic sum becomes the effective operate quantity, per the bias characteristic shown in Figure 8.

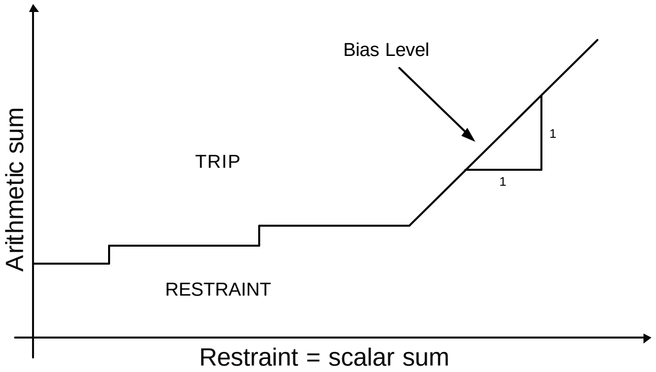


Figure 8. Bias Characteristic of Charge Comparison

The bias level is an operate threshold which provides security in the presence of spurious operate current due to line charging current, current transformer mismatch and other errors. As shown in Figure 8, the bias level rises sharply after the scalar sum reaches a high value. This provides security for unequal ct saturation during high current external faults. At lower currents, the bias level is much lower allowing for a high sensitivity without sacrificing security.

The operating principle of the charge comparison relay is very similar to that of a percentage differential current differential relay, but instead of comparing phasor quantities, the differential measurement is based on half-cycle charges. The local relay receives a current value equivalent to the positive half-cycle charge from the remote end (negative for the ground subsystem). This value is compared to the corresponding half-cycle charge in the local end. For an internal fault, they are both positive and the scalar and arithmetic sums are formed and compared to the operating criteria.

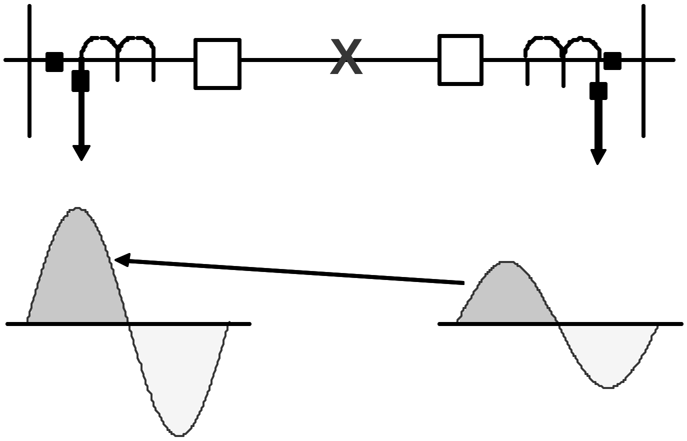


Figure 9. Charge Comparison Operation for Internal Fault

For an external fault, the received positive charge from the remote end coincides with the local negative charge and the relay restrains properly.

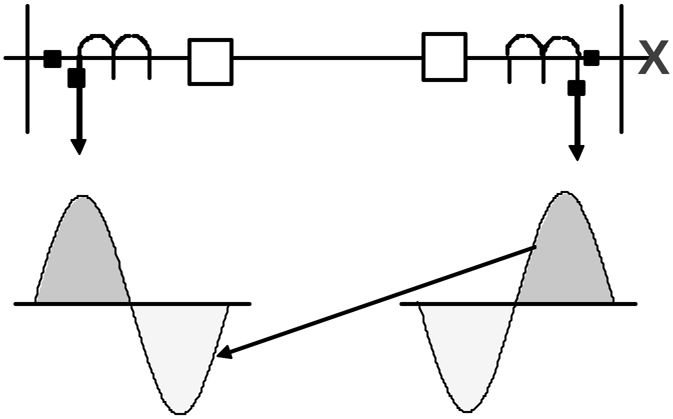


Figure 10. Charge Comparison Restraint for External Fault

In addition to the charge comparison function, the relay includes a complementary high speed element. This element's operating principle is similar to a phase comparison protection.

Setting Considerations

A current differential relay is very simple to set compared to a distance relay. While the distance relay is using the line impedance as a reference, the current differential relay is only interested in fault current levels on the protected line. The setting should be low enough to detect all types of faults on the line, and high enough to ensure that the relay does not operate for external faults in the presence of ct errors or other measuring errors.

Sensitivity

A relay needs to be set sensitive enough to detect all faults within its protective zone, but need not be more sensitive than that. If 100% of the faults in the protective zone are detected with a certain relay setting nothing is gained by further increasing sensitivity (with the possible exception of operating speed). On the other hand, increased sensitivity will decrease security.

For current differential relays, there has been a tendency to use the most sensitive setting the relay allows. This is done in order to ensure sufficient sensitivity with sufficient margin for measuring errors that may influence relay sensitivity. However, the increased sensitivity will sacrifice security and false trips for external faults may occur due to the same measuring errors that motivated increased sensitivity. The source and magnitude of these errors will be discussed later in this paper.

Electromechanical pilot wire relays generally recommended a pick-up setting of 50% of minimum fault current, the fault current being the sum of the currents from the two line ends. The 50% criterion was partly due to speed as electromechanical relays will operate faster for a higher current vs. setting and partly due to the need to allow for phase shifts in the fault currents due to different source angles. A digital current differential relay may or may not need to use the same safety factor depending on the measuring method used. For instance, the charge comparison relay is totally unaffected by phase shifts up to 90 degrees, and will maintain the same sensitivity within this range.

Using the same criterion for a current differential relay we find that the required sensitivity is:

$$\begin{aligned} &I_{op} > I_{min} + Restraint \\ &where \\ &I_{op} = \left| \overline{I}_{Lmin} + \overline{I}_{Rmin} \right| \\ &I_{min} = \text{set minimum operating threshold} \\ &Restraint = f(\overline{I}_{Lmin}, \overline{I}_{Rmin}) \end{aligned} \tag{6}$$

Note that the relay operates on the sum of the currents. The minimum fault current does not equal the minimum infeed current from one line end. Even with no infeed from one line end, the current differential relay will operate provided that the single infeed current fulfills the operating criterion.

This simple calculation will determine the setting required to detect all faults on the line. The minimum fault current will determine the I_{min} setting and the constants used for a settable restraint. Generally, the 50% setting rule applied for electromechanical relays is also used for numerical current differential relays so that the relay is set to operate for half the theoretical fault current. Any setting adjustments required for security considerations for charging current and ct errors will be discussed later, as well as weak infeed applications.

Dependability and Security

Dependability is the degree of certainty of correct operation in response to system faults while security is the degree of certainty that the relay will not operate incorrectly. Together these two terms define Reliability. Dependability and security are opposing elements and every design of a protection scheme is a compromise between the two.

The relay itself undergoes design criteria to optimize reliability by a suitable balance between security and dependability. The relay settings also influence security and dependability of the protective scheme. Increased sensitivity increases dependability but decreases security. Increased sensitivity may improve operating speed, but any gain in speed need to be weighted against loss of security. The settings need to balance dependability and security in order to maximize the resulting degree of reliability and provide adequate operating speed for the protection scheme.

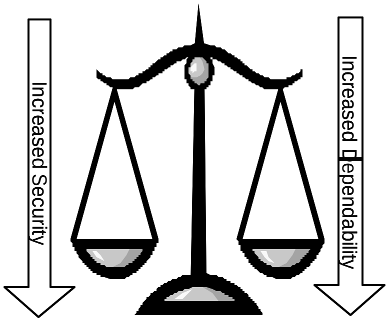


Figure 11. Security and Dependability

Sensitivity versus Operating Time

Conventional current-measuring relays have an inverse time/current characteristic with shorter operating time for higher multiples of applied current as compared to set operating threshold. Microprocessor relays may not display this dependency to the same degree and it may not be necessary to increase sensitivity to achieve high speed tripping. As the operating time depends on the relay design, the operating time curves for the selected relay need to be considered when high speed tripping is of importance for the application.

The charge comparison relay’s operating speed is largely independent of current magnitude versus pick-up setting when the threshold is exceeded by ¼ of an Amp.

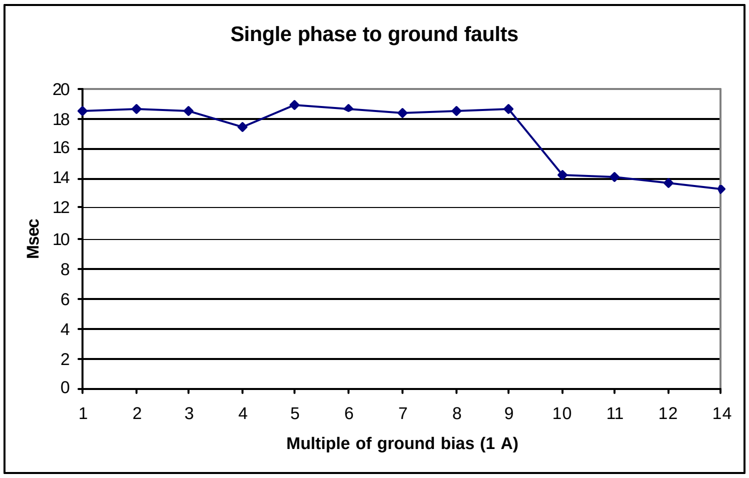


Figure 12. Ground Fault Operating Times

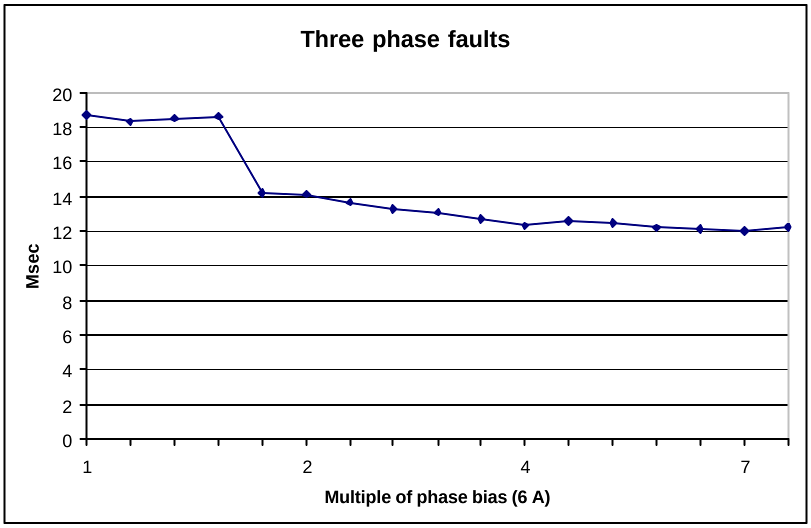


Figure 13. Three Phase Fault Operating Times

As evident from these operating time curves, there is little gained by increasing sensitivity. Tripping times for differential current of 0.25 amp over the bias will be essentially the same as differentials 4 or more times the bias setting. The shorter operating times at 10 times set ground bias and 1.8 times set phase bias reflect the operation of the high speed element. This element is 4 – 6 ms faster than the charge comparison, and provides faster triping for higher fault currents.

Weak Infeed Considerations

Weak Infeed is a term used for a condition when there is no or little fault current contribution from one line end for a fault on the protected line. A radial line with no source at the load end would be a typical example of a weak infeed terminal. Transmission line terminals may also exhibit weak infeed depending on system configuration at the time of the fault.

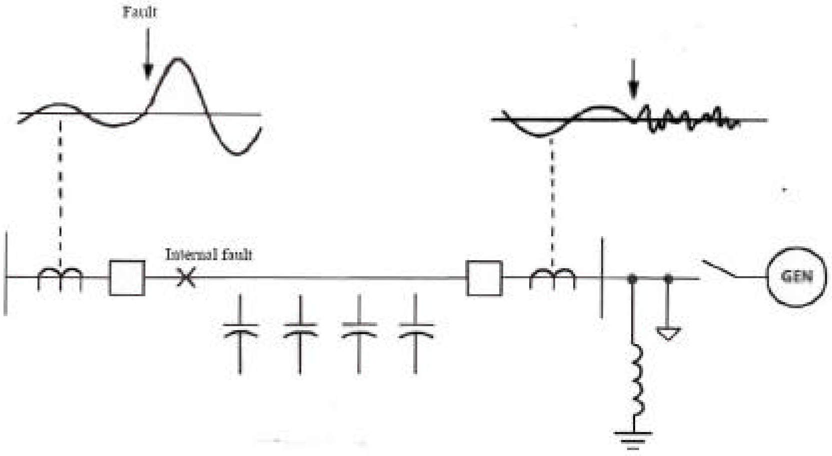


Figure 14. Weak Infeed Condition

Current differential relays are in general not affected by weak infeed conditions and has no or very simple logic for weak feed tripping. The current differential principle inherently trips for internal faults with weak infeed provided that the total fault current, whether fed from one or two line ends, is above the relay setting threshold.

A current differential relay operates on the sum of the currents. If $I_L + I_R >$ restraint, the relay will trip regardless if one of the terms is 0 or below the relay's minimum sensitivity. Whether the weak end will trip or not depends on the design of the relay system. Some current differential relays have supervision elements based on the local current magnitude. Others supervise with the summed current magnitude. Depending on the method used, a weak infeed logic may be needed to trip the line terminal with little or no fault current.

The charge comparison relay operates using 'normal charge comparison' as long as both infeed currents are at least 0.5 A rms. When the weak infeed current is below this threshold, the weak end sends a permissive Weak Current Message which enables the strong end to trip if $I_L >$ bias. The strong end then transfers a trip message to the weak end.

Charging Currents

Charging current is a capacitive leakage current on the transmission line. Unlike the load current, the charging current into one line end is not exiting the other. Clearly, the charging current will cause a differential current when comparing the currents in the two line ends.

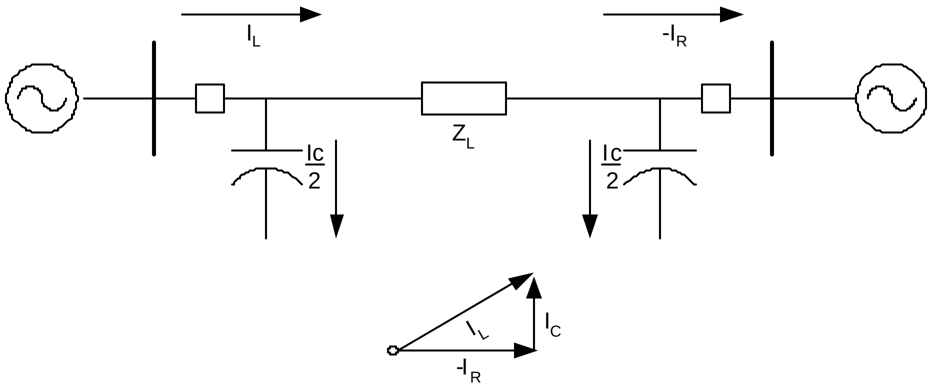


Figure 15. Line Charging Current

Many modern current differential relays have a charging current compensation feature. One method is by entering a term representing the charging current into the differential algorithm, subtracting this current from the local current. Charging current can be estimated by measuring line voltage and dividing by the set capacitive reactance.

It may be of interest see how useful such a feature is. We are presenting three examples:

- 115 kV line, 38 miles
- 500 kV line, 51.2 miles
- Cable, 16 miles, 23 kV

115 kV Line
This 38 miles long 115 kV line has the following data:

Shunt capacitive reactance	X'_{C1}=0.14 MΩ-mile
	X'_{C0}=0.20 MΩ-mile
	CT ratio = 1200/5 = 240

A rough approximation of capacitive reactance and resulting charging current is:

$$\begin{aligned} &X'_{C1} = 0.14 M\Omega mile \\ &I_{C1} = \frac{V_{line-neutral}}{X'_{C1}} \cdot miles = \frac{115000}{0.14 \cdot 10^6 \cdot \sqrt{3}} \cdot 38 A_{primary} = 18.02 A_{primary} = 0.08 A_{secondary} \\ &X'_{C0} = 0.20 M\Omega mile \\ &3I_{C0} = \frac{3 \cdot V_{line-neutral}}{X'_{C0}} \cdot miles = \frac{3 \cdot 115000}{0.20 \cdot 10^6 \cdot \sqrt{3}} \cdot 38 A_{primary} = 37.84 A_{primary} = 0.16 A_{secondary} \end{aligned} \tag{7}$$

With a differential bias setting of at least several Amps, we can see that the charging current for this overhead line is negligible and will have little affect the operation of a current differential relay whether compensated for or not.

500 kV Line
The 97 miles long 500 kV line has the following data:

Shunt capacitive reactance	xc1 = 235 MΩ-meter
	xc0 = 341 MΩ-meter
	CT ratio = 3000/5 = 600

The positive sequence charging current is estimated as:

$$\begin{aligned} &xc1 = 235 \text{ Mohm} - \text{meter} \\ &\text{L} = 97 \text{ miles} \\ &X'_{C1}(total) = \frac{xc1}{L(meters)} = \frac{235}{51.2 \cdot 1609} = 2851 \text{ ohms} \\ &I_{C1} = \frac{500000}{\sqrt{3} \cdot 2851} = 101 \text{ A primary } = 0.17 \text{ A secondary} \end{aligned} \tag{8}$$

And the zero sequence charging current:

$$\begin{aligned}
&xc0 = 341 \text{ Mohm} - \text{meter}\\
&\text{L} = 51.2 \text{ miles}\\
&X^{'}_{C0}(total) = \frac{341}{51.2 \cdot 1609} = \text{ 4135 ohms}\\
&3I_{C0} = \frac{500000}{\sqrt{3} \cdot 4135} = 70 \text{ A primary } = \text{ 0.12 A secondary}
\end{aligned} \tag{9}$$

With a differential bias setting of at least several Amps, we can see that the charging current for this overhead line is negligible and will have little affect the operation of a current differential relay whether compensated for or not.

Cables

For cables, the charging current could be large enough to have to be considered in the settings, unless a compensation feature is used in the relay. Generally, it is sufficient to increase the settings as cables often have sufficient minimum fault currents not to require very high sensitivity. In addition, many cable applications lack the potential transformers required for compensation, so the feature may be of no use.

Cable shunt capacitive reactance will be specified for the actual cable (calculated or measured), or can be taken from a table with typical cable data.

This example is for a 16 miles long cable with the following data:

Shunt capacitive reactance $X_{C1} = X_{C0} = 2070$ MΩ-mile

CT ratio = 800/5 = 160

$$\begin{aligned}
&X^{'}_{C1} = X^{'}_{C0} = 2070\,\Omega mile\\
&I_{C1} = 3I_{C0} = \frac{V_{line-neutral}}{X^{'}_{C1}} \cdot miles = \frac{23000}{2070 \cdot \sqrt{3}} \cdot 16 = 102.6A_{primary} = 0.64A_{secondary}
\end{aligned} \tag{10}$$

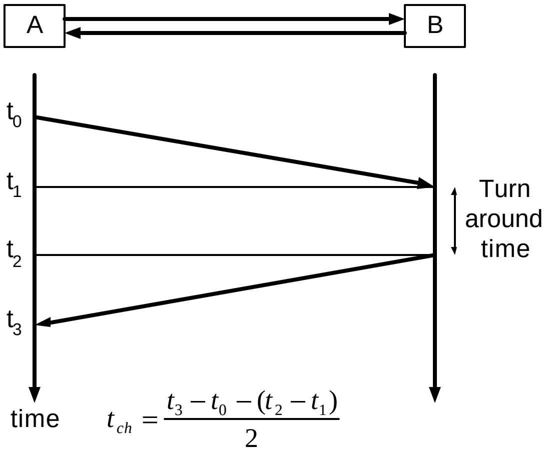
The charge comparison relay includes a 0.25 A safety margin for charging current, when the most sensitive setting is used. Any charging current above this should be taken into account by increasing the bias setting. For this case, phase bias and ground bias should add 1.0 A to the minimum setting of 1.0 A; the minimum recommended setting is thus 2 A. If sensitivity requirements have already determined that a higher setting is sufficient, no additional margin is required.

Communications Channel Delays

While there are differences between electromechanical pilot wire relays and microprocessor current differential relays fundamental relaying principles are still valid, regardless of how the implementation is made. A microprocessor relay basically performs the same function as its electromechanical predecessor. However, the difference in the communications link utilized is significant. The pilot relay is operating in real-time; the analog data from the remote line end is synchronous with the data in the receiving local end. A digital line current differential relay samples the currents, processes them and sends them over a digital communications link in digital format, resulting in a time delay with respect to the real-time samples at the receiving end.

This time delay is seen by the relay as a phase shift between local and remote current samples, and the phase difference is proportional to the channel delay. Pilot wire relays without any compensation feature can accept up to maximum 1 ms channel delay (representing a 22 degree phase shift) when used over digital communication media. Microprocessor current differential relays compensate for the channel delay by memorizing the local current samples until the remote end current quantities are received to properly align them in time.

To align the current data from the two line ends, the channel delay needs to be known. Most digital current differential relay designs have the ability of measuring and compensating for channel delay. Channel delay estimation is made by ping-pong measurement. The exact method and measurement frequency vary but the principle is similar. One end sends out a special message that is echoed back from the remote end. The loop time less the "turn-around" time divided by two is then the one-way delay.



$$t_{ch} = \frac{t_3 - t_0 - (t_2 - t_1)}{2}$$

Figure 16. Communications Channel Delay

The calculated one way delay is used by the relay to align the received current information with local, stored current measurement that was made one channel time delay period previously. As long as measured channel delay equals actual channel delay, there is not error (except small inherent errors due to the finite sampling frequency, timer resolution, accuracy, etc.).

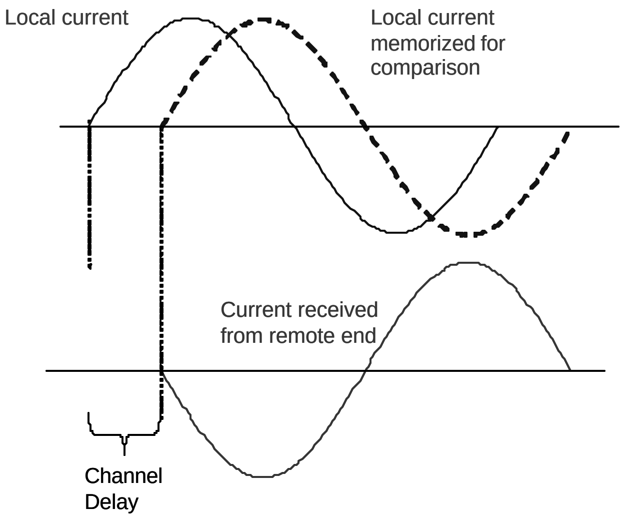


Figure 17. Channel Delay Compensation

When the actual delay deviates from measured delay, the error introduced to the relay will look like a differential current due to the apparent phase shift between the local and remote currents. Different relay designs deal with this condition in different ways. In general, measuring principles based on the phase relationship between the currents in the line ends are more tolerant to channel delay errors than measuring principles based on magnitude comparison.

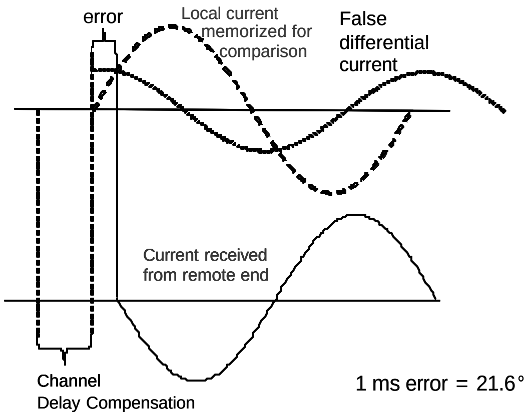


Figure 18. False Differential Current for 1 ms Channel Delay Error

Channel delay measurement by ping-pong can be made very accurately and will not introduce any significant error for current differential measurement. However, when using digital telecommunications networks there is a risk of asymmetrical delays being introduced. Telecommunications networks are designed with high redundancy and uses path switching. If the network is not designed to take relaying into account, the transmit path can take a different route over the network than the receive path and the channel delays will be unequal. An example of this is shown in Figure 19.

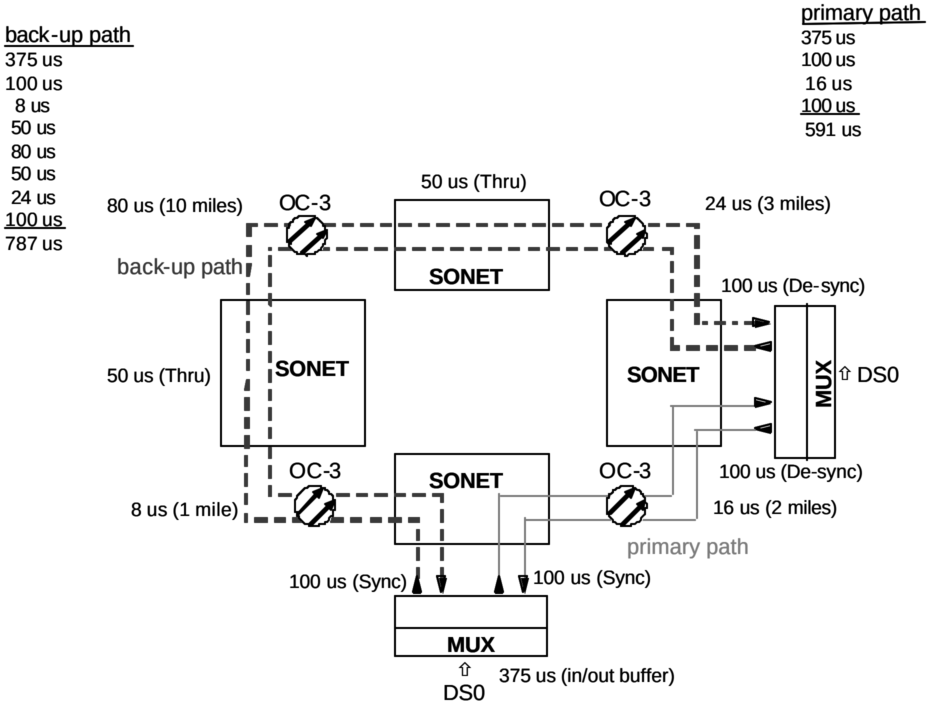


Figure 19. SONET Channel Delays

The example shows less than 0.5 ms difference is channel delays, and while this might be typical for small utility dedicated communications networks the asymmetric delays might become much larger if the network is tied to a higher order telecommunications network. Differences in the order of 2 – 3 ms are not uncommon if either the network is extensive (many nodes) or the fibers are very long.

The asymmetric delay is going to introduce an error for a relay using the ping-pong time delay measurement. The measured loop-time is divided by two and used as a one-way delay. The relay in one end will underestimate the channel delay by Δt and the other will overestimate with the same amount. The error Δt equals the difference between transmit and receive path delays divided by two.

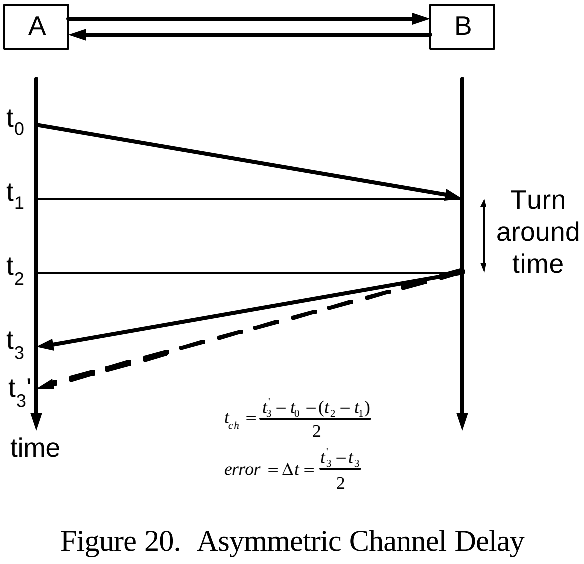


Figure 20. Asymmetric Channel Delay

The charge comparison relay was designed to be used over switched networks and elegantly handles channel delay asymmetry. The charge comparison 'nesting' process with comparing half-cycle charges inherently accepts +/- 4 ms channel delay error without any degradation in performance. Note that 4 ms error equals 8 ms *difference* in transmit and receive delays. The result is 100% correct as long as the right half-cycle charges are compared and there is no loss of sensitivity or security.

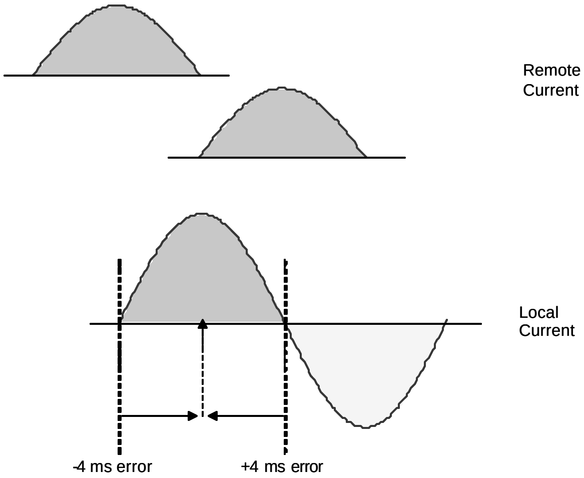


Figure 21. Charge Comparison (Internal Fault)

How much time delay error that can be tolerated for percentage differential relays depends on the settings and the design of the relay. A higher setting will give better tolerance for errors during external fault but will result in reduced sensitivity for internal faults. Channel delay errors during internal fault conditions will further reduce sensitivity. A theoretical estimate for channel delay error allowed can be made based on the operating and restraint characteristic but this does not take into account finite sampling frequency and other errors introduced due to filtering or channel time delay measurement. A typical recommended number for maximum channel asymmetry for percentage differential relays is 1 ms. Some relays offer GPS synchronizing options that can measure the one-way delays individually and will then correctly compensate for asymmetric channel delay.

CT Saturation

One source of ct measuring errors is ct saturation. CT saturation is less of a problem for internal faults, and the main concern is for external faults with unequal degree of saturation in the two line ends. When one of the ct's saturate, and not the other, the secondary currents presented to the relays will cause a differential current to be measured. Generally, ct errors due to saturation can be compensated by decreasing the relay sensitivity. Some percentage current differential relays include a ct saturation detector that increases the bias in the presence of saturated current waveforms. Other current differential relays, like the charge comparison, have a measuring principle that is inherently secure for ct saturation.

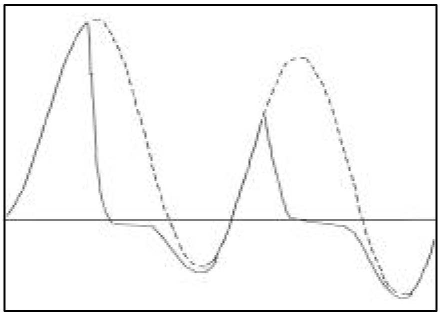


Figure 22. Primary (dashed) and Secondary (solid) Currents during CT Saturation

In addition to the external ct errors presented to the relay, the additional errors contributed by the relay itself needs to be considered. The main sources for these errors are the relay input transformers and the filtering technique used.

Input Transformers

The charge comparison relay has a patented design of the input transformers. The transformers faithfully reproduce the current input wave forms, with any dc offset and ct saturation by the use of a flux cancellation technique that creates a near perfect current transformer. The input transformer consists of a small toroidal core with a single turn looped through its center. This single turn is an extension of the secondary winding of the ct supplying the phase current waveform. An active circuit cancels out the flux in the toroidal core. This allows the toroid to handle large dc offsets without saturating. The circuit maintains its accuracy over a 250-ampere (rms) dynamic range. This patented procedure prevents any dc offsets that may be present in the current waveform from saturating the core.

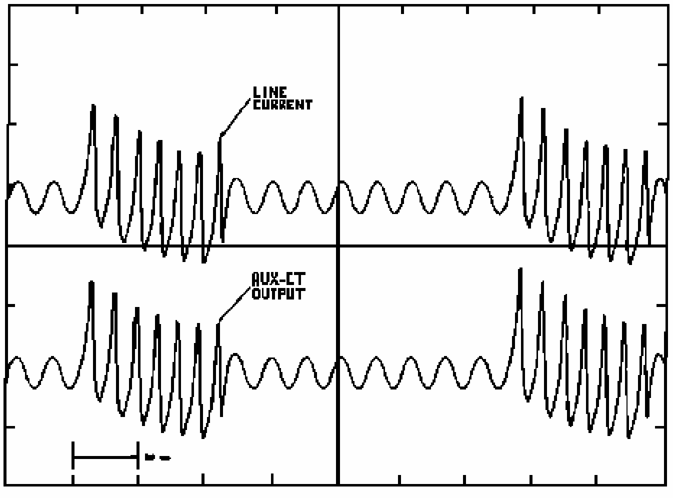


Figure 23. Response of Input Transformers

The upper waveform represents the current into the input transformer (LINE CURRENT). The lower waveform is the current out of the transformer (AUX-CT). The input transformer correctly reproduces the waveform, including dc offset.

Phasor Estimation at CT Saturation

Digital relays that compute phasors through a filtering process will exhibit erroneous current estimation due to ct saturation. The extent of the error depends on the filtering method used and the degree of saturation.

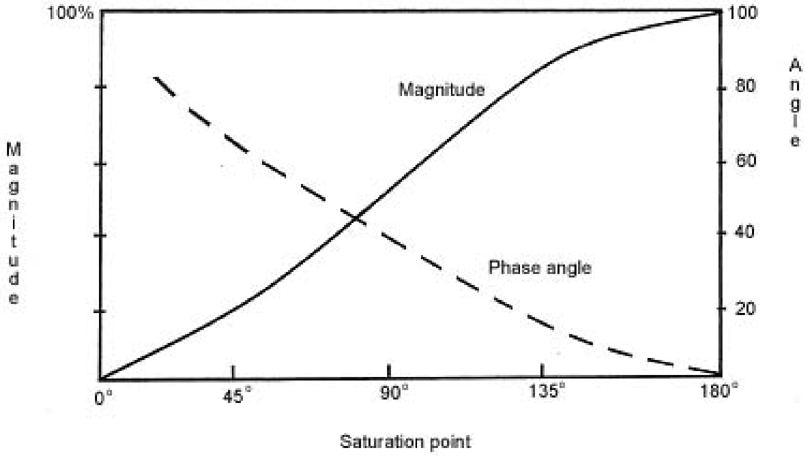


Figure 24. Filter Output for CT Saturation

Figure 24 depicts a typical response of a Fourier or cosine filter. The left axis shows how the magnitude is affected as a function of the saturation point on the x-axis. The later in the point in the cycle the saturation occurs, the lower the magnitude error. The right axis shows the phase angle shift of the computed phasor as a function of the saturation point. Again, the error decreases with the saturation point moving closer to the end of the half-cycle.

The phasor error's impact on any computed quantities in the relay should also be considered. If computed sequence currents are based on erroneous phase phasors, the resulting sequence phasor might display a proportionally higher error.

The effect of the filtering and corresponding setting adjustments required will depend on the actual relay and the manufacturer's recommendations for settings and ct dimensioning should be followed. In addition, the relay's input transformer's ability of correctly reproducing the ct currents may need to be taken into account.

Charge Comparison during CT Saturation

The charge comparison relay does not use phasor computation and the effect of ct saturation is not influenced by phasor errors. The actual sample values are used to calculate the half cycle charge used in the measuring algorithm.

The charge comparison measuring principle is very dependable and secure in the presence of ct saturation. To explain the operation, a couple of examples for internal and internal fault with ct saturation are presented.

Internal Fault with CT saturation

An internal fault with correct reproduction of the current in at least one line terminal is bound to provide sufficient differential current for reliable operation. The worst case for an internal fault is heavy saturation of both ct's.

The charge comparison operates by calculating the half-cycle charge. The design requires a half-cycle of at least 6 ms to be considered a valid value to be used in the charge comparison algorithm. Any half-cycles of less duration are discarded, and no current differential measurement is performed in either line end for this half cycle. If the ct saturates early so that the 6 ms half-cycle wave form is not provided, there is a risk that tripping for internal faults would be delayed. The relay overcomes this possible short-coming by a complementary high speed element using a phase comparison operating principle.

The high speed element has a higher operating threshold as ct saturation is not a problem for lower fault currents. High speed operation requires only 2 ms sample values above the threshold to initiate a trip. Figure 25 shows an example with saturation in one line end only, but the same operation will take place even with both ct's saturated for an internal fault. The scheme's security for external faults with ct saturation is not compromised as the high speed logic requires that the other line end has currents above a certain threshold as well. In case the fault is external, the two currents will be in phase and trip conditions will not be fulfilled.

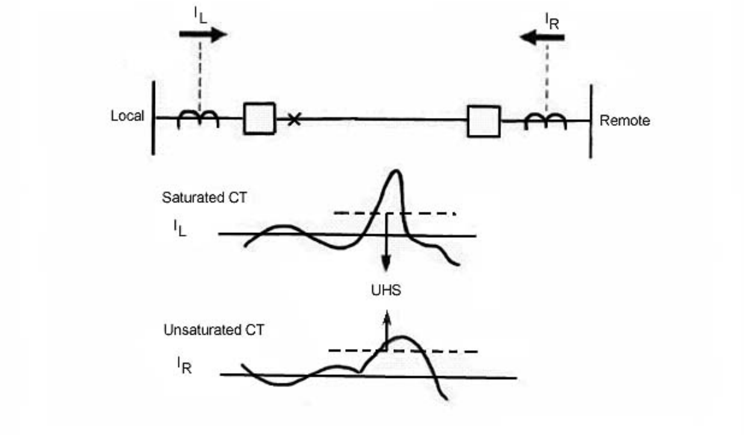


Figure 25. Internal Faults with CT saturation

External Fault with CT saturation
Figure 26 illustratres the waveforms from a heavily saturated ct for a three-phase fault.

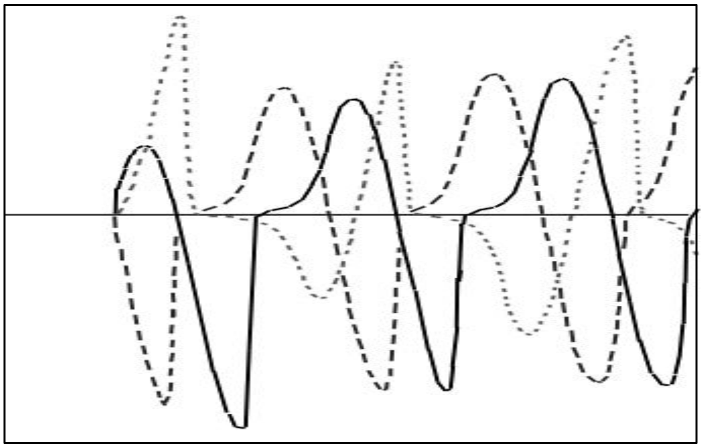


Figure 26. CT Saturation for a Three Phase Fault

Assuming that the ct's in the other end do not saturate, a considerable differential current will be measured by the relays. For the charge comparison relay, two different scenarios present themselves:

- Saturated half-cycle waveforms < 6 ms
- Saturated half-cycle waveforms > 6 ms but < 10 ms

The first case is handled by the logic that does not base any comparison on a current with less than 6 ms half-cycle duration between zero crossings and the relay restrains properly. In addition, any half-cycle with a pulse width larger than 10 ms will be rejected by the ct saturation supervision detector (also called dc offset filter) and disregarded in the same way. This means that the most critical case is when the ct saturation provides at least a half-cycle of 6 ms before ct saturation but with low enough dc offset not causing the unsaturated ct to produce a half-cycle of more than 10 ms duration.

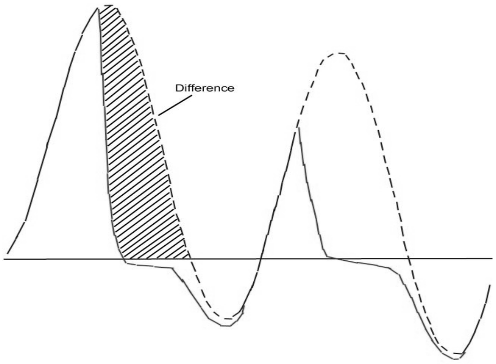


Figure 27. Left Side Saturated, Right Side Unsaturated

Assuming that the secondary current provides at least one half-cycle of 6 ms (130 degrees) before the point of saturation, the 'missing charge' in the saturated portion of the half cycle would be significant and seemingly cause misoperation. However, the charge comparison reverts to a type of phase comparison principle at currents above 16 A (peak). This means that any contribution from current samples above 16 A are ignored and the current samples contributing to the charge calculation will never exceed 16 A. It can be show that the maximum 'equivalent' rms error will never exceed 8.5 A.

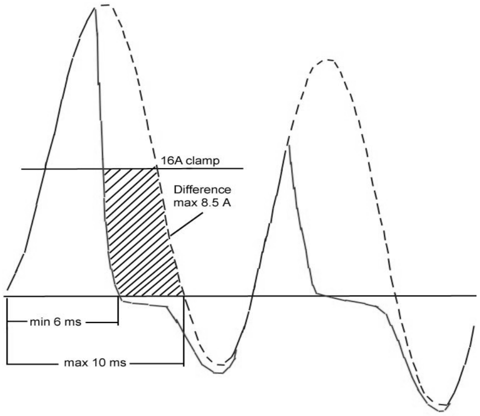


Figure 28. Maximum Charge Error

This does not mean that bias needs to be set above 8.5 A. While the relay uses a fixed bias for low currents, it converts into a percentage bias slope for currents above 20 A where ct saturation could occur. For example, with a setting of 2 A bias and a total fault current of 40 A (which is still a low current for ct saturation) the effective bias for the relay is 2 + 20 A = 22 A. The 8.5 A error will not produce misoperation.

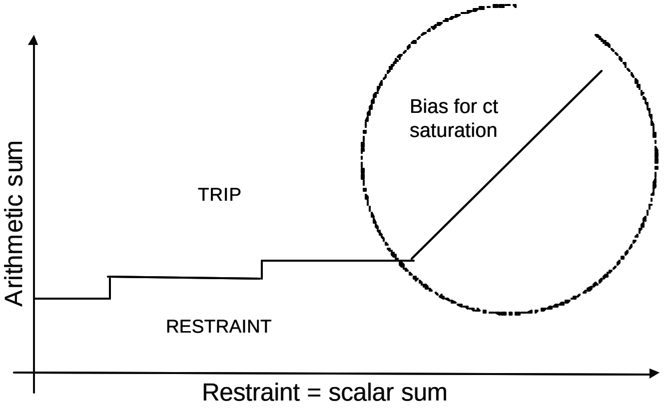


Figure 29. Percentage Slope for CT Saturation Errors

One additional concern could be the behavior of the ground element for heavily saturated ct's during a three phase fault. Summing the three phases will result in an erroneous current. However, this current will not resemble a 60 Hz waveform, and the short current pulses will not fulfill the 6 ms requirement. Even with higher set sensitivity for the ground element, it remains stable.

Figure 30 illustrates the ground current resulting from the very heavily saturated phase currents illustrated in Fig 26. It can be seen that even for this extreme case, the 6 ms limit is not fulfilled and no misoperation will occur.

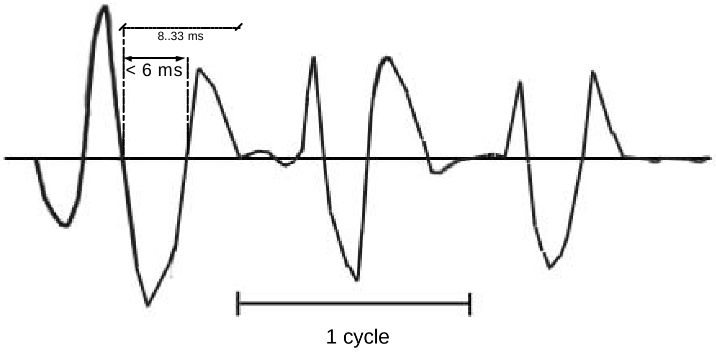


Figure 30. Resulting Ground Current for Three Phase CT Saturation

Two phase faults do not produce much zero sequence if the two phases saturate somewhat similar.

Other CT Errors to Consider

One cause of ct saturation that is less obvious is energizing of a transformer. A very common application for current differential relays is the configuration shown in Figure 31. The transformers are typically energized by closing breaker L and significant inrush current flows on the line.

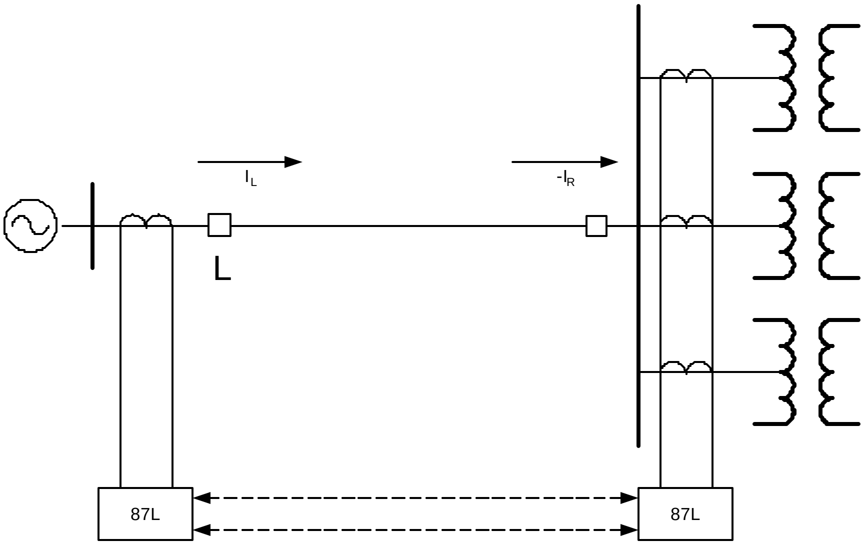


Figure 31. Transformer Energizing

The current waveforms for an energizing event are shown in Figure 31 (Local) and Figure 32 (Remote). The distorted waveforms are typical for transformer energizing. Note that the current magnitude is low. At first glance, the Local and Remote currents look the same, and 180 degrees apart. The transformers are external to the current differential protective zone and all current entering the line in L is also leaving it at R. However, a more detailed analysis shows that this is not the case.

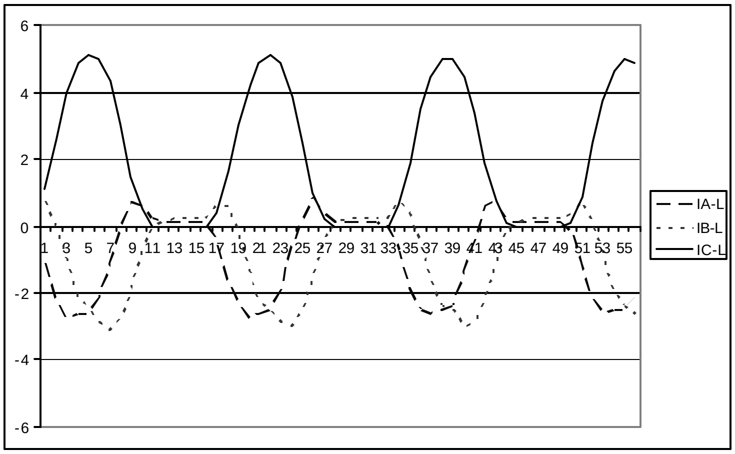


Figure 32. Local Currents

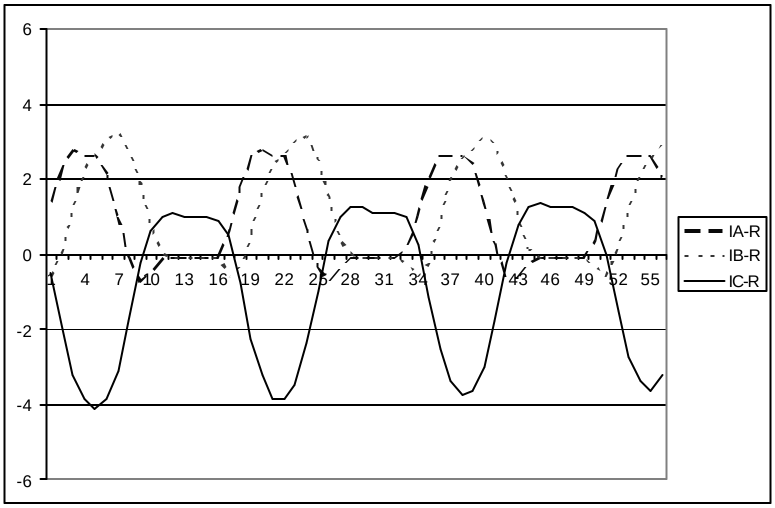


Figure 33. Remote Currents

There is a considerable difference between phase C secondary currents in the two line ends. The 'error' is produced in the remote end, where the transformers are located. At this line end, several ct's are paralleled. The nature of magnetizing current, being fully offset, could cause excessive ct exciting current even for relatively small current magnitudes. The exciting current is a dc component and would explain the resulting dc-displacement in the affected phase.

The difference is small if measured in 'equivalent' A rms, but may cause misoperation for a current differential relay set with much too high sensitivity.

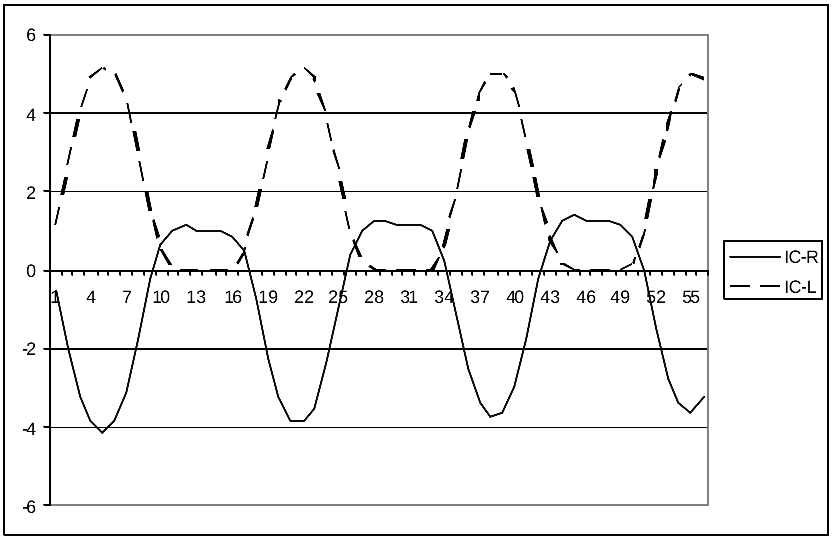


Figure 34. DC displacement for transformer energizing

The charge comparison relay did experience false tripping for this application when phase bias was set to 1.0 A. The obvious remedy was to increase the setting, and the application did not require such a high sensitivity. In addition, a ‘ct saturation detector’ (also called dc-offset filter) was developed for the charge comparison relay that efficiently prevents misoperation for this type of application even with the most sensitive settings applied in the relay.

Conclusions

- Current Differential Protections are easy to set as the operation depends on fault current levels only.
- Actual fault current levels as determined by a fault study should be used to determine setting parameters. To use the minimum setting is rarely required.
- Current Differential Line Protection Relays should be set sensitive enough to detect all faults on the protected line, but need not be more sensitive than that.
- Too high sensitivity compromises security. Measurement errors generally affect security much more than dependability. It is recommended to use the highest setting that ensures operation for all faults on the line.
- The effect of CT saturation and other ct errors on relay settings needs to be considered for the actual relay as different filtering designs and input transformer designs will behave differently for these conditions. Use of excessive sensitivity should be avoided.
- When applying the relay over a switched digital communications network, the relay’s ability to handle asymmetric channel delays may need to be reviewed and settings adjusted accordingly.

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Biographies

Solveig M. Ward

Solveig received her M.S.E.E. from the Royal Institute of Technology, Sweden in 1977. The same year she joined ABB Relays. She has held many positions in Marketing, Application, and Product Management. Assignments include a six-month period in Montreal, Canada and two years in Mexico. When Ms. Ward returned to Sweden, she was responsible for the application aspects in the development of a numerical distance protection relay and in charge of marketing the product. After transferring to ABB in the US 1992, she was involved in numerical distance protection application design, and was Product Manager for ABB's line of current differential and phase comparison relays. Solveig has written, co-authored and presented several technical papers at Protective Relaying Conferences. She is a member of IEEE-PSRC Main Committee and holds one patent.
In 2002, Solveig joined RFL Electronics Inc. as Director of Product Marketing. She is presently involved in the development of new products.

Tim Erwin

Tim Received his B.S.E.E.T from the New Jersey Institute of Technology in 1996. The same year he joined RFL Electronics Inc. He has held positions as Sr. Customer Service Engineer for the RFL 9300 Charge Comparison relay, Customer Service Supervisor, Sr. Sales Engineer and Sr. Applications Engineer. Tim is currently in the position of Protection Product Engineer and is involved in the development of new products.